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2280 HV Rijswijk (ZH)  
☎ +31 70 340 2040  
TX 31651 epo nl  
FAX +31 70 340 3016

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**03290424.5**

Der Präsident des Europäischen Patentamts;  
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets  
p.o.

**R C van Dijk**

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ALCATEL  
54, rue la Boétie  
75008 Paris  
FRANCE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:  
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.  
If no title is shown please refer to the description.  
Si aucun titre n'est indiqué se référer à la description.)

Circuit for programmable stepless clock shifting

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The present invention relates to a circuit for programmable stepless clock shifting.

In many electronic applications, for example digital CDRs (Clock Recovery Unit), it is required to generate a clock signal with a programmable phase shift with respect to a reference clock.

In a number of situations, when transferring data between different chips, boards or devices, the associated clock is usually not distributed. The main reason is pin count reduction and power saving. At the receiving end, the problem of recovering the associated clock arises, in order to sample and process the incoming data stream. The operation of phase aligning often cannot be avoided also when the associated clock signal is distributed along with the data signal.

It is possible to design a clock recovery circuit working without a reference clock under precise assumptions on the data pattern and the local VCO frequency tuning range. Since these hypothesis is often not met in the applications, the known solutions mainly require a reference clock frequency within a well defined tolerated range.

A number of known techniques are already available for generating a clock signal with a programmable phase shift, namely delay locked loops (DLL), phase locked loops (PLL), open loop delay lines, digital phase aligners (DPA).

PLL based solutions require considerable power and chip area and are generally not able to cope with a wide range data transition density or long CID (continuous identical digits) sequences, as often required by applications. Often a PLL is used to generate N phases of the reference clock. They are all distributed to each receiving macro in which one is selected in order to sample the incoming data. This solution requires a lot of area for the wiring. Besides, switching noise, variations in phase difference between the clock multiphases and duty cycle distortion become a challenging issue when covering a long path; in addition the minimum distance in degrees between two adjacent phases is limited by the technology used for the chip.

In other proposed schemes, one PLL is used to generate one filtered clock phase which is then distributed to all the receiving macros. Locally all the phases are generated by means of a DLL. Power consumption and occupation

area remain a severe issue. Also in these cases the minimum distance in degrees between two adjacent phases is limited by the technology.

Cases in which the multi-phase clock is generated by means of an open loop delay line are also known. In this schemes, power consumption (all the phases are generated also if not used) is an issue. Moreover the whole algorithm is complicated because the phases do not cover  $360^\circ$  and the phase spacing is PTV (process, temperature and supply) dependent and limited.

Solutions that delay the data (digital phase aligners, DPA) are also known. The main drawback is that the delay chain length is supposed to cover the jitter tolerance amplitude and not only the clock period, which results in longer delay chains. This implies more eye closure and again a PTV dependent and limited phase spacing. Moreover, an architecture that delays the data requires the local availability of the exact transmitter clock frequency.

Therefore in view of the known solutions, that are not quite efficient, it is the main object of the present invention to provide a circuit for programmable stepless clock shifting solving all the above mentioned problems.

The basic idea of the present invention is to provide a programmable stepless clock shifter, consisting of a splitter generating a  $0^\circ$  and a  $90^\circ$  shifted clocks from a reference clock, and an interpolator of this two phases, which provides at the output the desired pre-set clock phase.

These and further objects are achieved by means of a method and circuit as described in the attached claims, which are considered an integral part of the present description.

The invention will become fully clear from the following detailed description, given by way of a mere exemplifying and non limiting example, to be read with reference to the attached drawing figures, wherein:

- Fig. 1 shows a block diagram of the circuit in accordance with the invention.

As shown in fig. 1, the solution consists of two blocks in series, a splitter (SPLITTER) and an interpolator (INTERPOLATOR): the splitter receives a clock CK\_REF and generates two clock phases,  $90^\circ$  shifted; the interpolator uses these two clock phases and two coefficients SIN\_ $\Phi$  and COS\_ $\Phi$ , and produces a clock, which has a phase that depends only on the input coefficients.



A detailed description of the two blocks is given in the following.

SPLITTER. The input clock CK\_REF is summed (in the adder S1) and subtracted (in the subtractor S2) to a delayed clock CK\_DEL supplied by a delaying circuit DEL. It is possible to show analitically or graphically that the two  
 5 clocks at the outputs of S1 and S2 are 90° shifted for construction, independently on the value of delay  $\Delta$  as soon as the following condition on the delay is met:

$$\Delta \neq \pi + k\pi, \quad k = \{0, \pm 1, \pm 2, \dots\}$$

This means that the vectorial product of the input clock CK\_REF and the  
 10 delayed clock CK\_DEL should not be zero. In the applications this condition is easily met.

Typically the value of  $\Delta$  is  $90^\circ \pm 50\%$ .

When the input clock CK\_REF and the delayed clock CK\_DEL are orthogonal, that means shifted exactly by 90° each other, the output amplitudes  
 15 of S1 and S2 are equal. In the other cases two squarers SQ1 and SQ2 are encharged to output two clocks CK\_90 and CK\_0 with the same amplitude. In practice in the circuit implementation the two squarers are ever present to ensure output amplitude uniformity.

INTERPOLATOR. This block receives the two 90° shifted clocks CK\_90  
 20 and CK\_0 from the splitter and provides a clock with a phase that is programmable by setting two appropriate input coefficients.

The working principle relies on the following trigonometric relation:

$$\sin(\omega t + \Phi) = \sin(\omega t)\cos\Phi + \cos(\omega t)\sin\Phi$$

By summing two 90° shifted clock phases,  $\sin(\omega t)$  and  $\cos(\omega t)$ , with  
 25 appropriate coefficients,  $\cos\Phi$  and  $\sin\Phi$ , it is possible to obtain any delayed version  $\sin(\omega t + \Phi)$ , of the input reference clock  $\sin(\omega t)$ .

In the circuit the two 90° shifted clocks CK\_90 and CK\_0 are sent to respective inputs of two multipliers M1 and M2; the second input of M1 is supplied with a first coefficient SIN\_ $\Phi$  and the second input of M2 with a second  
 30 coefficient COS\_ $\Phi$ .

The outputs of M1 and M2 are supplied to the inputs of an adder S3 wich gives at the output the wanted clock reference CK\_REF\_ $\Phi$  with the pre-set phase difference  $\Phi$  with respect to the input clock CK\_REF.

The two coefficients  $\text{SIN}_\Phi$  and  $\text{COS}_\Phi$  are selected in any wanted way. For example they can come from a memory table TAB suitably addressed, according to the wanted phase shift  $\Phi$ , which can be any.

The advantages of the present invention are clear.

5 The minimum angle between two adjacent phases is not technology nor temperature nor supply dependent. The resolution can be chosen as high as needed (stepless clock shifter).

The solution is open loop, so it does not require a careful design of the loop in order to grant stability. When used in CDRs, no minimum data transition  
10 density has to be defined.

A monolithic chip implementation, for example a VLSI technology, takes advantage of the low power consumption and the low silicon area required. No filter has to be implemented.

Further implementation details will not be described, as the man skilled in  
15 the art is able to carry out the invention starting from the teaching of the above description.

Many changes, modifications, variations and other uses and applications of the subject invention will become apparent to those skilled in the art after considering the specification and the accompanying drawings which disclose  
20 preferred embodiments thereof. All such changes, modifications, variations and other uses and applications which do not depart from the spirit and scope of the invention are deemed to be covered by this invention.

## Claims

1. Circuit for programmable stepless clock shifting, characterized in that it comprises:

- a splitter (SPLITTER), receiving a clock reference (CK\_REF) and generating two 90°-shifted clock phases (CK\_0, CK\_90);
- 5 - an interpolator (INTERPOLATOR) receiving said two 90°-shifted clock phases (CK\_0, CK\_90) and two coefficients (SIN\_Φ, COS\_Φ), and supplying a programmable phase clock (CK\_REF\_Φ), which has a phase shift with respect to said clock reference (CK\_REF) that depends only on said two coefficients (SIN\_Φ, COS\_Φ).

10 2. Circuit according to claim 1, characterized in that said splitter (SPLITTER) comprises:

- a delay circuit (DEL) receiving said clock reference (CK\_REF) and supplying a delayed clock (CK\_DEL);
- an adder (S1) and a subtractor (S2) of said clock reference (CK\_REF)
- 15 and said delayed clock (CK\_DEL), supplying at the output said two 90°-shifted clock phases (CK\_0, CK\_90).

3. Circuit according to claim 2, characterized in that said splitter (SPLITTER) further comprises at the output two squarers (SQ1, SQ2) of said two 90°-shifted clock phases (CK\_0, CK\_90), so as the latter have the same

20 amplitude.

4. Circuit according to claim 2, characterized in that the delay (Δ) introduced by said delay circuit (DEL) is typically  $\Delta = 90^\circ \pm 50\%$ , and is

$$\Delta \neq \pi + k\pi, \quad k \in \{0, \pm 1, \pm 2, \dots\}$$

5. Circuit according to claim 1, characterized in that said interpolator (INTERPOLATOR) comprises:

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- a first and second multiplier (M1, M2) respectively receiving one of said two 90°-shifted clock phases (CK\_0, CK\_90) and a first and second coefficient (SIN\_Φ, COS\_Φ);
- an adder (S3) receiving the outputs of said first and second multiplier
- 30 (M1, M2) and supplying said programmable phase clock (CK\_REF\_Φ).

6. Circuit according to claim 5, characterized in that said first and second coefficient (SIN\_ $\Phi$ , COS\_ $\Phi$ ) have a value of respectively  $\sin\Phi$  and  $\cos\Phi$ , such that the following relationship is performed:

$$\sin(\omega t + \Phi) = \sin(\omega t)\cos\Phi + \cos(\omega t)\sin\Phi$$

5 where  $\Phi$  is said programmable phase of the programmable phase clock (CK\_REF\_ $\Phi$ );

$\sin(\omega t + \Phi)$  is the frequency of said programmable phase clock (CK\_REF\_ $\Phi$ );  
 $\sin(\omega t)$  and  $\cos(\omega t)$  are the frequencies of said two 90°-shifted clock phases (CK\_0, CK\_90).

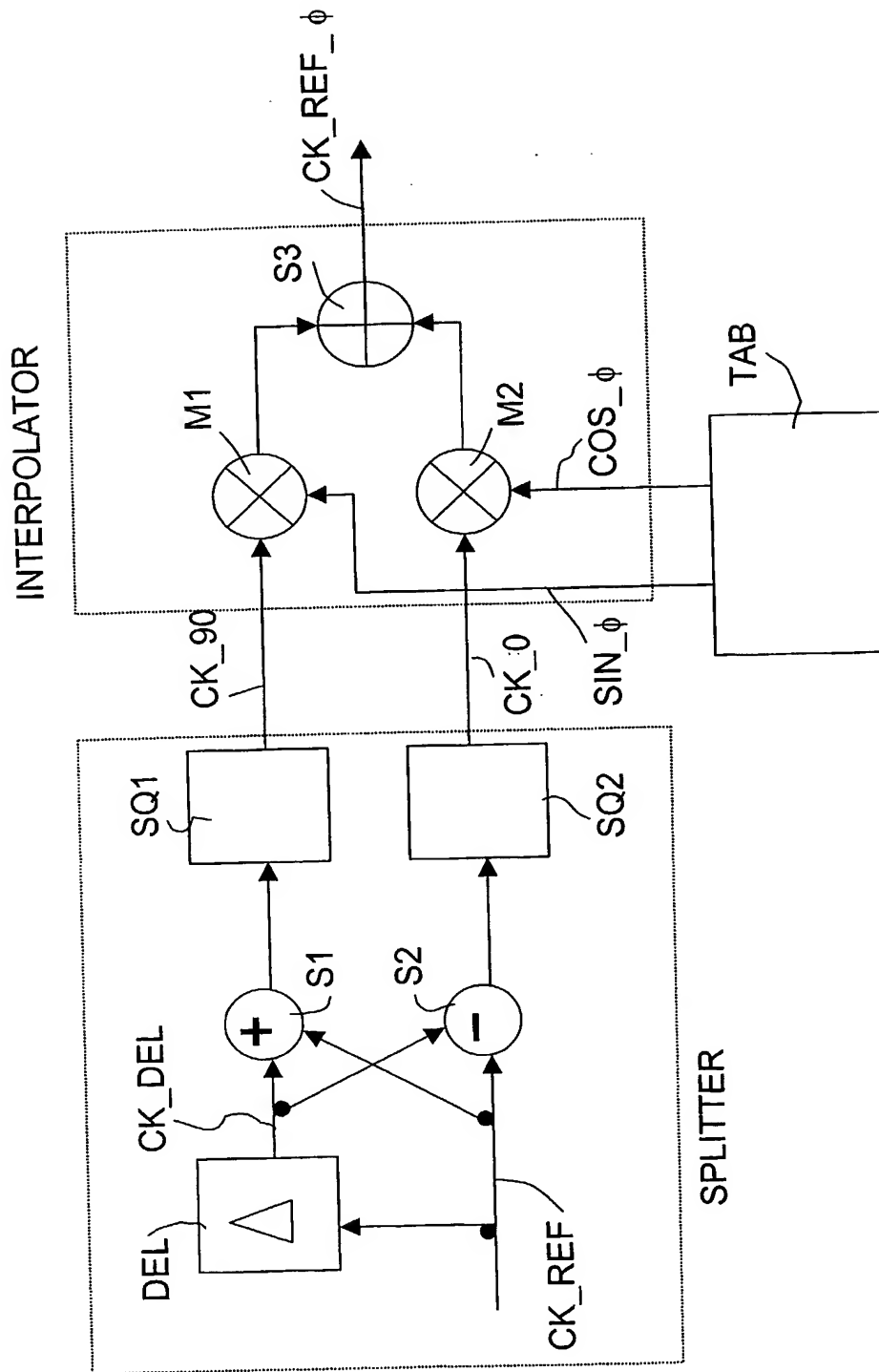
10 7. Circuit according to claim 5 or 6, characterized in that said first and second coefficient (SIN\_ $\Phi$ , COS\_ $\Phi$ ) are selected from a memory table (TAB), addressed according to the wanted programmable phase ( $\Phi$ ).

## Abstract

### Circuit for programmable stepless clock shifting

The present invention provides for a circuit for programmable stepless clock shifting, consisting of a splitter generating a  $0^\circ$  and a  $90^\circ$  shifted clocks from a reference clock, and an interpolator of the two shifted clocks, which provides at the output the desired pre-set clock phase.

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**FIG. 1**

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